REMARKS/ARGUMENTS

In the Office action dated March 9, 2005, Examiner rejected claims 1, 2, 7, 8, and 15 under 35 U.S.C. 102 (b) as anticipated by Marz (USPN 5,923,706), and claims 1-4, 7-12 and 15 under 35 U.S.C. 102 (e) as anticipated by Naudet (USPN 6,377,644). Claim 14 was rejected under 35U.S.C.103 (a) over Naudet (USPN 6,377,644).

Examiner stated that claims 5, 6, 13, 16 and 17 would be allowable if re-written in independent form. However, applicant has not re-written the claims since he believes that the base claims are allowable in view of the arguments presented below.

Applicant appreciates the time and consideration provided by Examiner in reviewing this application. Applicant carefully reviewed the Examiner's comments and respectfully traverses the rejection of the claims 1-4, 7-12, 14-15 at least for the following reasons.

Anticipation under 35 U.S.C. 102 requires that each and every claimed feature be disclosed by a single prior art reference. Therefore, the references relied upon by the Examiner in rejecting claims 1-4, 7-12, 14-15 must disclose articles that are reasonably identical to the claimed inventions.

US Patent No. 5, 923,706

Marz describes a method that uses a 'predetermined clock' which is set to a multiple of **the expected frequency of the incoming signal**. This is not a 'predetermined frequency offset' as described in the method of the present application.

A 'predetermined clock' described in Marz's method is a clock running at a fixed and predetermined frequency. Furthermore Marz explains that this clock frequency must be of a high frequency so that it can be divided down to the same frequency as the signal being measured. This means that it is an integer multiple of the signal being measured. To be able to produce the same accuracy as the method of the present application (0.01 multiplied by the clock period), the Marz method would require a 'predetermined clock' running at 100 times the input signal.

In contrast, the present method **does not require the use of high frequency clocks** as mentioned in the preamble of the present application. An advantage of this is that lower frequency clocks are relatively cheap.

The present method does not use an integer multiple of the input signal frequency. Instead it relies on the reference being offset by a non-integer ratio (such as 100/101) so that there is a 'strobe' effect between the reference and input signals.

Claim 1 – '706, Column 1, Lines 59- Column 2, Line 4

The method described in the present application detects the 'first occurrence of a predetermined phase relationship' and the 'subsequent occurrence of the predetermined phase relationship'. Any variations in this are used to determine the phase jitter. These variations can only occur at the rate set by the frequency offset and then only at the end of each sample period.

The Marz's method adjusts the phase of the reference clock by suppressing some of the high frequency clocks (see column 4 lines 58 to 64). This adjustment is performed for each phase variation. Therefore what Marz proposes is to continually try to maintain phase alignment. The Marz method does not 'detect the first and subsequent occurrence of a phase relationship'. Instead it adjusts the reference frequency to maintain a stable relationship.

Claim 1 - '706, Column 2, Lines 5 - 16

Marz states that the comparison (reference) clock is 'formed' so that it has a 'phase relationship' to the 'modified clock signal'. This indicates that the reference clock is adjusted to maintain a fixed phase relationship to the input. In contrast, the method of the present application does not attempt to alter or 'track' the input signal; instead it determines phase jitter by measuring the number of clock cycles it takes for the first and subsequent occurrence of phase alignment (phase relationship). When jitter is present this will be different from the calculated (ideal) value. The maximum – minimum count is the amount of jitter.

Claim 1 - '706, Column 2, Lines 17 - 29

The action of adjusting the reference clock to maintain a stable phase relationship is once again described. It is clearly stated in the present application that "An important advantage of the process according to the present invention is that the predetermined clock signal is brought to a defined phase relationship to the data signal ..."The method disclosed in Marz clearly requires the reference clock to be adjusted to maintain a stable phase relationship. This is completely teaches away from the method claimed in the present application.

Claim 2 - '706, Column 6, Lines 20 - 30

These lines relate to the operation of timers. There is no reference to measuring or generating the reference clock.

Claim 15

Although Marz's patent is a method of measuring jitter in telecommunication PCM systems, the present application describes a different and unique method of measuring jitter in a telecommunications PCM signal.

The Marz's method uses a high frequency clock, which is then 'adjusted' to maintain a consistent phase match with the input signal. The frequency adjustments are produced by the

suppression of some of the clock pulses. The adjustments produce a ramp which is then demodulated to produce an analogue signal which can then be used to determine the jitter on the input signal.

The present invention, however, uses a reference clock, which is chosen so that it will naturally produce a phase strobbing effect so that then reference and input signal will only have the same phase relationship once every '*n*' cycles of the reference clock. Where the ratio of the reference clock to input signal is ***n:m*** and wherein *m* & *n* are the lowest integers. If the ratio is 100/101 then it will take 100 reference clock cycles (101 input clock cycles) for the phase relationship to match. The present method detects the 'first occurrence of a predetermined phase relationship', such as both rising edges occurring at exactly the same time. Counting of the number of clock cycles for 'the subsequent occurrence of a predetermined phase relationship' (the same phase relationship) then commences. This is repeated a plurality of times, using the same starting point. The maximum/minimum of all readings is used to determine the amount of jitter.

Another key difference is that there is no analogue circuitry in the apparatus of the present invention: this is another key difference between the arrangement described in Marz that uses comparators, demodulators, integrators and sample-and-hold circuits.

In view of the above, Applicant respectfully submits that Marz's patent clearly teaches away from the present invention, and the claims as originally filed are novel over Marz.

Rejection based on US Patent US 6,377,644

Claim 1 - '644 Column 1, Lines 5 – 9

The method described in Naudet's patent uses a frequency offset. This is described as 'a ratio of integers'. Although this appears to be similar to the requirements of the present invention, the implementation/use of the clock is completely different. The method described in Naudet requires the clock signal to be fed via a delay line chain so that effectively a multiple of clock signals are produced with a fixed phase offset or delay. The present invention, to the contrary, uses a standard single phase clock as explained at Column 3, Lines 45 to 52 of the description.

Claim 1 - '644 Column 1, Lines 63 - 65

The Examiner states that the measurement period, and hence the sampling clock, should be such that an integer number of samples should be taken over each of the signal clock periods. This means two things: firstly the circuit requires a high frequency or multiphase clock (specifically stated as not required by the present method); and secondly it is the input signal that is being sampled (the present invention does not employ sampling at all). The reason for the sampling in Naudet is so that a standard Digital Signal Process (DSP) can be performed on the samples. This method implements normal DSP

techniques and does not 'directly' measure the jitter in a similar manner – using digital circuits - to that employed by the present invention.

Claim 1 - Column 3, Lines 62 to Column 4, Line 1

The description refers to the first sample of many samples, and is not the 'first occurrence of a phase relationship' as described in the present application. The description then goes on to describe the way the phase changes and therefore how the samples change. Further reading shows that these samples are stored and passed to a calculating (processing) unit so that a Fourier transform can be performed on them. There is no direct readout from the system. This method is basically a Digital Signal Processing (DSP) circuit applying a digital filter to the signal so that the phase jitter can be calculated, and clearly teaches away from the present invention.

Claim 1 - '644 Column 4, Lines 1 - 10

This feature relates to how the samples produce a 'periodic sequence' which can then be subjected to a Fourier transform to determine the frequency of the input signal. In contrast, the present invention does not take samples. Furthermore the present invention does not store samples, nor does it use a calculating unit or perform any Fourier transforms. Therefore what Naudet describes is completely different to anything done by the present invention. In Naudet, Figure 3A shows how samples are related to the clock (CK) and not to the input signal. There is no indication in Naudet that direct phase relationship between the reference frequency, used to take the samples, and the input signal are compared or the result of a comparison being used.

Claim 1 - '644 Column 4, Lines 64 - 67

Figure 4A in Naudet shows how the input signal moves with respect to the samples. This is to be expected with jitter even if the sample clock (CK) is an integer multiple of the nominal input frequency. It does not however *indicate a first, second or any other occurrence of a specific phase relationship between the reference and the input signal.* For this to relate to a phase relationship the diagram would have to show the correct phase relationship, a variation in the phase and then the relationship being re-established. This is clearly shown in Figures 2 and 3 of the present application.

Claim 2 - '644 Column 6, Lines 20 - 30

This describes a method of producing a clock frequency from a voltage controlled oscillator. The most important part is the sampling circuit which produces a set of phase shifted clocks all derived from the same source clock. In contrast, the present invention does not use a voltage controlled oscillator or produce or use multiple phases of any clock. There is no resemblance between this circuit and the method used in the present invention.

Claim 2 - '644 Column 6, Lines 31 - 47

This describes the method of adjusting the frequency of the voltage controlled oscillator. However, as already explained, the frequency of this oscillator is set so that it is 'a ratio of integers' of the input signal, not a fixed frequency offset as used in the present invention. The use of a voltage controlled oscillator is very common for frequency synchronisation circuits and is in fact the heart of a standard Phase Locked Loop (PLL) circuit, so this in itself is not new. Furthermore, the present invention does not include such a circuit. The method described in the present application requires the input frequency to be measured and the reference frequency to be set. Naudet requires the period AND the phase to be adjusted to match the input signal. The phase is specifically excluded from the present invention as it is impossible to have a fixed frequency offset that can allow a complete phase match. Naudet clearly teaches away from the present invention.

Claim 3 - '644 Column 5, Lines 1 - 14

Naudet aligns the reference (sampling) clock with the input signal and then compares the samples of that clock with the samples of the next/subsequent clock sample. This is quite different to the present method, in that signals are not aligned, neither are clock samples compared. Moreover, in the present invention there is no comparison of any actual phase between the reference clock and the input clock. The present invention detects a fixed (predetermined) phase relationship (first occurrence) and then counts the number of reference clock cycles for this phase relationship to re-occur (subsequent occurrence). **It is the variation in this number that the present invention uses in order to determine the amount of jitter.**

Claim 3 - '644 Column 5, Lines 6 - 28

Naudet refers to a method of taking samples at a rate much higher than both the reference clock AND the input signal. *The method of the present application uses a much lower rate with the input signal divided down to a lower ratio.*

Claim 4 - '644 Column 5, Lines 15 - 28

The cited section of Naudet's patent states that input signal can first be sampled so that the position of the edges in this signal can be determined. This allows the system to determine the nominal frequency of the input signal. Claim 3 of the present application states that the frequency offset of the reference clock can be adjusted so that the circuit can detect jitter of a fixed frequency that could be masked if it is 'beating' with the measurement period. The Naudet patent does not include anything for adjusting the reference frequency so that the circuit is able to detect fixed frequency jitter. It is submitted therefore that the devices to which these sections refer are not the same.

Claim 4 - '644 Column 5, Lines 49 - 59

The calculation quoted in this section is a calculation on the expected phase ('which enables a calculator to determine whether the phase of signal S_{in}, with respect to the considered measurement period T, is the expected phase or not'). No check for maximum or minimum is suggested, and although it could be argued that a calculation could include maximum and minimum, it is not expressly included. Further to this, the maximum and minimum of a phase jitter is dependent on the total offset from the 'expected instant in time' and therefore it requires a complete knowledge of the position of where the phase relationship should be.

Claims 7, 8, 11, 12

This is dependent on the rejection of the previous claims and therefore if the above arguments are accepted then these claims would be valid.

Claim 9 - '644 , Figure 6, 3 & 4 and Column 6, Lines 59 - 67

Although Box 6 is a counter and it does feed into Box 4, which is a microprocessor, the description makes it clear that it is not a frequency counter. The description is 'the microprocessor records from counter 4 *the number of errors* enabling to reconstitute the shape of the signal S_{in} according to Figure 3B, then to measure its frequency. The overall effect is to measure frequency. However, the method used is completely different to a frequency counter. The counter holds samples of the 'errors' which it appears are then subject to a Fourier analysis to determine the frequency that would produce these errors. If it was a frequency counter then the input signal S_{in} would be used to clock the counter, however, the diagram clearly shows that the counter is clocked every time there is a rising (or falling) transition on the sampled signal. This is clearly not a frequency counter and the frequency is being determined by some 'clever mathematics' as indicated by the description where it states 'the microprocessor records from counter 4 the number of errors enabling to reconstitute the shape of the signal S_{in}'.

Claim 10 - '644 Column 6, Lines 38 – 47

This claim does call for a programmable oscillator, as does the Naudet patent. The difference, however, is in the requirement. The claim refers back to claim 8 and its use for producing a reference with a predetermined offset, which has been clarified earlier.

Claim 15 - '644, Column 1, Lines 5 - 9

The difference in this claim is the method used and again the reference back to claim 7.

Claim 14

Claim 14 is dependent upon allowable claim 7, and should be allowed.

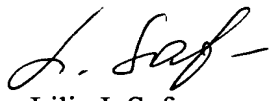
Thus, claims 1-4, 7-12 and 14 and 15 are distinguishable from Naudet and should, therefore, be allowed.

Applicant respectfully submits that claims 1-17 pending in the present application are allowable over the prior art and the application is in condition for allowance. Favourable reconsideration of rejection of the claims pending in this application is respectfully solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 during its entire pendency, or credit any overpayment, to Deposit Account No. 06-1135. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, other-wise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1135.

Respectfully submitted,

FITCH, EVEN, TABIN & FLANNERY

By: 

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